Press Release

PX5 RTOS Simplifies Development of 64-bit Hard Real-Time Applications with Support for IAR Embedded Workbench for Arm

Integrated support satisfies the growing demand for Asymmetric Multiprocessing (AMP) and Symmetric Multiprocessing (SMP) capabilities by global IoT manufacturers.

SAN DIEGO, CA—June 12, 2023—PX5, a global leader in high-performance real-time operating systems and middleware, today announced hard real-time Asymmetric Multiprocessing (AMP) and Symmetric Multiprocessing (SMP) support for the 64-bit Arm architecture integrated with the IAR Embedded Workbench® for Arm® development environment. This new support brings unprecedented load balancing and security features to hard real-time applications and complements existing PX5 RTOS Arm support for the 32-bit Cortex-M, Cortex-R, and Cortex-A architectures.

"Many applications that demand hard real-time and deterministic processing require capabilities well beyond those of embedded Linux, the most popular operating system for Arm 64-bit architectures," said William Lamie, CEO, PX5. "With the growing demand for very high-performance AMP and SMP applications, like video processing and cellular modem, the PX5 RTOS hard real-time support promises to unleash the full performance and security benefits of Arm's 64-bit Cortex architectures to meet the most demanding hard real-time designs."

"The combination of IAR Embedded Workbench for Arm and PX5 maximizes the potential of development teams working with highly complex hard real-time systems," said Lotta Frimanson, Director of Product Management at IAR. "Our long-standing relationship with Bill Lamie and PX5 demonstrates our commitment to helping developers expedite deployment of AMP and SMP applications and reduce development risks."

Dynamic Load Balancing

The hard real-time AMP and SMP support provided by the PXR RTOS includes dynamic pairing of ready application threads with available cores, enabling developers to concentrate on the application logic rather than a distribution of the workload across multiple processors. The PX5 RTOS SMP also allows the application to designate which cores each thread can execute on using several new APIs for setting and retrieving pre-thread processor affinity.

Pointer/Data Verification (PDV) Technology for 64-bit Arm

The PX5 RTOS patent-pending Pointer/Data Verification (PDV) technology constitutes an integral part of an overall defense-in-depth strategy, by helping to detect and mitigate both accidental and malicious memory corruption of function pointers, function return addresses, internal system objects, and memory pools. Without PDV, memory corruption could go unnoticed and function pointer or stack corruption could open the door to remote execution attacks.

Purpose-Built RTOS for Today's Demanding IoT Devices

The industrial-grade PX5 RTOS is an advanced, fifth-generation RTOS designed for the most demanding embedded applications with best-of-class size, performance, safety, and security. The PX5 RTOS is built on a native implementation of the industry-standard POSIX pthreads API, including semaphore, mutex, and message queues, and offers real-time extensions such as event flags, fast queues, tick timers, and memory management. This industry-standard support instantly enables a wide range of software stacks—both open source and commercial—for real-time embedded IoT platforms, reducing time-to-market, improving device firmware quality, and enhancing portability across platforms. Such benefits help device makers to maximize their investments in firmware development.

About PX5:

Headquartered in San Diego, CA, PX5 offers the industry's most advanced runtime solutions for deeply embedded applications. PX5 products include full source code and are available free of run-time royalties. For more information, please visit www.px5rtos.com or e-mail info@px5rtos.com.

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